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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/739,419	12/18/2003	Walter Lee Snyder	INTCP008	1288

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EXAMINER	
FIEGLE, RYAN PAUL	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/739,419	SNYDER, WALTER LEE	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claims 1-4 state that shadow registers are present in all of the execution units while the disclosure and figures show the shadow registers only being in the integer unit.

Based on the specification, figures and subsequent claims, the examiner believes that the applicant intended to form the claims as the rest of the application but misworded it. Correction is required.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the shadow registers being in each execution unit must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 and 13-21 are rejected under 35 U.S.C. 103(a) as being obvious over Arora et al. (US Patent 6,629,232).

4. As per claim 1:

Arora teaches a system comprising:

a plurality of execution units (Figure 3, items 130), each of said execution units having one or more data registers and one or more shadow registers, each shadow register being communicatively coupled to at least one data register in another

execution unit (column 3, lines 56-66) (The execution units' local copy of the register file contains data registers. These registers are also shadow registers for the other cluster since they contain remote copies of that cluster's copy of the register file.);

a memory unit (Figure 3, item 110); and

a control unit operable to issue control signals to the execution units, the control signals being operable to facilitate processing of data read from the memory unit, and to enable data transfers between the execution units (column 3, lines 26-29; Figure 3, item 321) (Since the steering logic determines which cluster get which instructions, it facilitates data read from the memory unit and enables data transfers between the EXUs).

Arora does not disclose the execution units ***including*** the data and shadow registers. Rather, Arora shows these registers outside the EXUs. However, such would have been obvious to one of ordinary skill in the pertinent art since including the registers within the execution units cuts down on register latency and power usage.

Further, it has been found by In re Dulberg (289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961)) that making parts separable is an unpatentable difference.

5. As per claim 2:

A system as in claim 1, in which each shadow register is connected to an input to a data register, such that data written to the data register is also written to the shadow register (column 3, lines 56-66; Figure 3).

6. As per claim 3:

A system as in claim 1, in which the plurality of execution units include one or more integer execution units and one or more datapath execution units (column 2, lines 48-51) (Arora defines execution unit as anything that sends or receives data from a register file. An ALU and datapath are encompassed by this definition).

7. As per claim 4:

A system as in claim 2, in which the data register comprises an accumulator register (It is obvious that a multiply-accumulate instruction will accumulate a result in a data register thus making it an accumulator. Multiply-accumulate instructions and their benefits are well known in the art) (Official Notice).

8. As per claim 5:

Arora also teaches a system comprising:

a control unit (column 3, lines 26-29; Figure 3, item 321);

a first execution unit, the first execution unit having a first data register; and

a second execution unit, the second execution unit having a second register containing a copy of the first data register's contents, the second register being communicatively coupled to an input of the first data register (column 3, lines 56-66).

Arora does not disclose the execution units ***including*** the data and shadow registers. Rather, Arora shows these registers outside the EXUs. However, it has been found by In re Dulberg (289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961)) that making parts separable is an unpatentable difference.

9. As per claim 6:

The system of claim 5, in which the first execution unit comprises a datapath execution unit (column 2, lines 48-51) (Arora defines execution unit as anything that sends or receives data from a register file. An ALU and datapath are encompassed by this definition).

10. As per claim 7:

The system of claim 5, in which the second execution unit comprises an integer execution unit (column 2, lines 48-51) (Arora defines execution unit as anything that sends or receives data from a register file. An ALU and datapath are encompassed by this definition).

11. As per claim 8:

The system of claim 6, in which the second execution unit comprises an integer execution unit (column 2, lines 48-51) (Arora defines execution unit as anything that sends or receives data from a register file. An ALU and datapath are encompassed by this definition).

12. As per claim 9:

The system of claim 7, in which the first execution unit comprises an integer execution unit (column 2, lines 48-51) (Arora defines execution unit as anything that sends or receives data from a register file. An ALU and datapath are encompassed by this definition).

13. As per claim 10:

The system of claim 5, in which the first data register comprises an accumulator register (It is obvious that a multiply-accumulate instruction will accumulate a result in a

data register thus making it an accumulator. Multiply-accumulate instructions and their benefits are well known in the art) (Official Notice).

14. As per claim 13:

A method comprising:

at a first execution unit, calculating a first result;

storing the first result in a first data register at the first execution unit; and

transferring the first result from the first execution unit to a first shadow register in a second execution unit (Arora: column 3, lines 56-66).

15. As per claim 14:

The method of claim 13, in which the acts of storing the first result in the first data register and transferring the first result to a first shadow are performed during the same clock cycle (Arora: column 3, lines 56-66; Figure 3) (The writes are done in parallel on the same wire).

16. As per claim 15:

The method of claim 13, further comprising:

at a third execution unit, calculating a second result;

storing the second result in a second data register at the third execution unit; and

transferring the second result from the third execution unit to a second shadow register in the second execution unit (column 3, lines 22-29) (The two clusters are shown for illustration, three clusters could be used, or alternatively a different EXU from the second cluster could write a result. Both would fulfill the limitations of the claim).

17. As per claim 16:

The method of claim 15, in which the act of transferring the first result from the first execution unit to the first shadow register is performed during the same clock cycle as the act of transferring the second result from the third execution unit to the second shadow register (Arora: column 3, lines 56-66; Figure 3) (The writes are done in parallel on the same wire).

18. As per claim 17:

The method of claim 15, in which the act of transferring the first result from the first execution unit to the first shadow register is performed at a frequency independent of the act of transferring the second result from the third execution unit to the second shadow register (Reoccurrence of instructions using the same destination registers is irregular; therefore, the writing will inherently be at different frequencies).

19. As per claim 18:

The method of claim 13, further comprising:

at the second execution unit, calculating a second result;

storing the second result in a second data register at the second execution unit; and

transferring the second result from the second execution unit to a third shadow register in a third execution unit (column 3, lines 22-29) (The two clusters are shown for illustration, three clusters could be used, or alternatively a different EXU from the second cluster could write a result. Both would fulfill the limitations of the claim).

20. As per claim 19:

The method of claim 13, in which the first execution unit comprises a datapath execution unit and the second execution unit comprises an integer execution unit (column 2, lines 48-51) (Arora defines execution unit as anything that sends or receives data from a register file. An ALU and datapath are encompassed by this definition).

21. As per claim 20:

The method of claim 13, in which the second execution unit comprises an integer execution unit and the first execution unit comprises an integer execution unit (column 2, lines 48-51) (Arora defines execution unit as anything that sends or receives data from a register file. An ALU and datapath are encompassed by this definition).

22. As per claim 21:

The method of claim 13, in which the second execution unit comprises a datapath execution unit and the first execution unit comprises a datapath execution unit (column 2, lines 48-51) (Arora defines execution unit as anything that sends or receives data from a register file. An ALU and datapath are encompassed by this definition).

23. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gadre (US Patent 6,308,253), and further in view of Arora.

24. As per claim 11:

Gadre teaches a system comprising:

a general purpose processor (Gadre: column 6, lines 47-49; Figure 4, item 102);

a memory unit (Gadre: Figure 4, item 134);

a user interface (Gadre: Figure 1, item 32); and

a plurality of special-purpose processors (Gadre: column 2, lines 64-67; column 3, lines 1-5) (In addition to doing general tasks, each core can do digital signal processing) comprising:

a plurality of datapath units (Gadre: column 6, lines 50-51), each of said datapath units including a data register;

an integer unit (Gadre: Figure 4, item 106; column 2, lines 64-67) (It does RISC functions),

a control unit operable to issue control signals to the integer unit and the datapath units (Gadre: column 7, lines 31-34).

Gadre does not teach the integer unit including one or more shadow registers, each shadow registers being communicatively coupled to a data register in a datapath unit, which Arora does (Arora: column 3, lines 56-66).

Arora's method cuts down on the number of ports in a register file and thus cuts down on register file latency (Arora: column 1, lines 46-63).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Arora to Gadre would cut down on register file latency.

25. As per claim 12:

The system of claim 11, in which the plurality of processors form part of a chip designed in accordance with a reconfigurable (Gadre: column 2, lines 64-67) (The controller is programmable) communications (Gadre: Figure 1) architecture.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 12-8.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan P Fiegle
Examiner
Art Unit 2183

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